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Title: FLASH CELL FUSE CIRCUIT

# **AMENDMENTS TO THE CLAIMS**

- 1. (currently amended) A memory device, comprising:
  - an array of floating-gate memory cells, each memory cell located at an intersection of a word line and a local bit line;
  - a first transistor having a first source/drain region coupled to a first supply potential node, a second source/drain region coupled to a latch input node, and a gate coupled to a first control node;
  - a second transistor having a first source/drain region coupled to the latch input node, a second source/drain region coupled to a first local bit line, and a gate coupled to a second control node; and
  - a fuse latch having an input coupled to the latch input node and an output coupled to an output node.
- 2. (original) The memory device of claim 1, wherein a first source/drain region of a first floating-gate memory cell is coupled to the first local bit line, a second source/drain region of the first floating-gate memory cell is coupled to a second potential node, and a gate of the first floating-gate memory cell is coupled to a first word line.
- 3. (original) The memory device of claim 2, wherein a first source/drain region of a second floating-gate memory cell is coupled to the first local bit line, a second source/drain region of the second floating-gate memory cell is coupled to the second potential node, and a gate of the second floating-gate memory cell is coupled to a second word line.
- 4. (original) The memory device of claim 2, wherein the first local bit line is coupled to a data line of the memory device through a data path.
- 5. (original) The memory device of claim 1, wherein each floating-gate memory cell is an n-channel floating-gate field-effect transistor.
- 6. (canceled)

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- 7. (original) The memory device of claim 1, wherein the second transistor is an n-channel field-effect transistor.
- 8. (canceled)
- 9. (currently amended) The memory device of claim 1 8, wherein the supply potential is in the range of approximately 1.65V to 2.0V.
- 10. (currently amended) The memory device of claim 2, wherein the second potential node is coupled to receive a potential lower than the potential of the first supply potential node.
- 11. (original) The memory device of claim 2, wherein the second potential node is coupled to receive a ground potential.
- 12. (original) The memory device of claim 1, wherein the fuse latch includes a pair of reverse-coupled inverters.
- 13. (currently amended) The memory device of claim 1, further comprising:

  a latch driver circuit capable of setting an output value of the fuse latch without regard to,

  and without disturbing the data value of, the <u>a</u> first floating-gate memory cell.
- 14. (original) A memory device, comprising:
  - an array of floating-gate memory cells, each memory cell located at an intersection of a word line and a local bit line;
  - a first transistor having a first source/drain region coupled to a first potential node, a second source/drain region coupled to a latch input node, and a gate coupled to a first control node;
  - a second transistor having a first source/drain region coupled to the latch input node, a second source/drain region coupled to a first local bit line, and a gate coupled to a second control node;
  - a third field-effect transistor having a first source/drain region coupled to a third potential node, a second source/drain region coupled to an output node, and a gate;

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- a fourth field-effect transistor having a first source/drain region coupled to the output node, a second source/drain region coupled to a fourth potential node, and a gate;
- a fuse latch having an input coupled to the latch input node and an output coupled to the output node;
- a first logic circuit having an output coupled to the gate of the third field-effect transistor,
  a first input coupled to a third control node, and a second input coupled to a fourth
  control node; and
- a second logic circuit having an output coupled to the gate of the fourth field-effect transistor, a first input coupled to the third control node, and a second input coupled to the fourth control node.
- 15. (original) The memory device of claim 14, wherein the third potential node is coupled to receive a supply potential.
- 16. (original) The memory device of claim 14, wherein the third potential node is coupled to receive the same potential as the first potential node.
- 17. (original) The memory device of claim 14, wherein the fourth potential node is coupled to receive a potential lower than the potential of the third potential node.
- 18. (original) The memory device of claim 14, wherein the fourth potential node is coupled to receive a ground potential.
- 19. (original) The memory device of claim 14, wherein the fourth potential node is coupled to receive the same potential as the second potential node.
- 20. (original) The memory device of claim 14, wherein the first logic circuit deactivates the third field-effect transistor and the second logic circuit deactivates the fourth field-effect transistor when a control signal from the third control node has a first logic level, and wherein the first logic circuit and the second logic circuit are responsive to a control signal from the fourth control node to selectively activate either the third field-effect transistor or the fourth field-effect transistor when the control signal from the third control node has a second logic level.

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- 21. (original) The memory device of claim 20, wherein the third field-effect transistor is a p-channel field-effect transistor, the fourth field-effect transistor is an n-channel field-effect transistor, the first logic level of the control signal from the third control node is a logic low level, and the second logic level of the control signal from the third control node is a logic high level.
- 22. (original) The memory device of claim 20, wherein the first logic circuit includes a NAND gate having a first input coupled to the third control node and a second input coupled to the fourth control node.
- 23. (original) The memory device of claim 20, wherein the second logic circuit includes a NOR gate having a first input coupled to the third control node through an inverter and a second input coupled to the fourth control node.
- 24. (original) The memory device of claim 14, further comprising:
  - a NOR gate having an output coupled to the third control node, a first input coupled to receive an enable signal, and a second input; and
  - a NAND gate having an output coupled to the second input of the NOR gate and having a plurality of inputs each coupled to receive an address match signal.
- 25. (original) The memory device of claim 14, further comprising:
  - a first NOR gate having an output coupled to the third control node, a first input coupled to receive a first enable signal, and a second input;
  - a NAND gate having an output coupled to the second input of the first NOR gate and having a plurality of inputs each coupled to receive an address match signal; and
  - a second NOR gate having an output coupled to a third control node of another fuse circuit, a first input coupled to receive a second enable signal, and a second input coupled to the output of the NAND gate.
- 26. (original) The memory device of claim 25, wherein the second enable signal is the binary complement of the first enable signal.

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27. (original) The memory device of claim 14, wherein the memory device is coupled to a processor.

- 28. (new) A memory device, comprising:
  - an array of floating-gate memory cells, each memory cell located at an intersection of a word line and a local bit line;
  - a p-channel field-effect transistor having a first source/drain region coupled to a first potential node, a second source/drain region coupled to a latch input node, and a gate coupled to a first control node;
  - a second transistor having a first source/drain region coupled to the latch input node, a second source/drain region coupled to a first local bit line, and a gate coupled to a second control node; and
  - a fuse latch having an input coupled to the latch input node and an output coupled to an output node.